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On the two-port network analysis of common amplifier topologies

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SUMMARY

Using two-port network transmission parameters, we derive exact expressions for the voltage/current gains and the input/output impedances of common amplifier topologies. The derived expressions are valid both for BJT and MOS-based amplifiers and are independent of any particular small signal transistor model. Copyright © 2009 John Wiley & Sons, Ltd.

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1. INTRODUCTION

Two-port network analysis techniques form a basic part of any elementary textbook in circuit theory [1] and are relatively old and well-established techniques [2]. Despite their noticeable value in offering black-box representations of any given circuit, neither elementary electronic circuits textbooks [3, 4] nor advanced ones [5, 6] offer more than a few demonstrative examples, if any, when it comes to two-port analysis of amplifiers. The reason may simply be that in deriving a two-port model for an amplifier, it is necessary to use common circuit analysis techniques such as mesh and nodal analysis applied on a small signal equivalent model of the amplifier. As the amplifier structure and topology change so does its equivalent model and hence analysis has to be repeated to derive a different two-port network which thus offers limited advantage to the two-port network analysis technique and renders it computationally inefficient [7–12].

In this work, we propose a significantly different approach in favour of two-port network analysis based on using the transmission matrix $[a]$. Here, we show in particular that the change in representation from one amplifier topology to the other can be confined to a change in input port

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and output port variables (V_1, I_1, V_2, I_2) *without changing the transmission matrix parameters* of the core active element. Accordingly, given the $[a]$ matrix for a BJT transistor, an MOS transistor or indeed any other active device, the derived expressions remain unchanged when expressed as functions of the four matrix coefficients. This may prove useful particularly with deep submicron technologies where transistor models have become considerably sophisticated and obtaining a reasonable equivalent circuit, using which mesh and nodal analysis can be used to analyze an amplifier topology is difficult. However, the effects of such sophisticated models on the performance of any particular amplifier topology can be easily obtained using the formulae proposed in this paper without amplifier re-analysis. We derive general expressions for the voltage/current gains and the input/output impedances in terms of the matrix elements for the well-known common-(emitter/source), common-(base/gate) and common-(collector/drain) topologies. Note that since our approach is independent of the active device which will actually be used to implement the amplifier, the historical notations common-(emitter/source), common-(base/gate) and common-(collector/drain) lack generality and need to be changed. We propose the alternative notations common-A, common-B and common-C instead. Based on our two-port analysis approach, which offers a higher level of abstraction, we also propose a novel differential amplifier structure based on the common-B topology and demonstrate further the use of the proposed technique in analyzing multiple-stage amplifiers and other non-amplifier cells such as a current mirror and a Darlington pair composite.

2. TWO-PORT AMPLIFIER TOPOLOGIES

In what follows, we describe a two-port network using the transmission parameters defined as (see Figure 1(a)) [13]

$$\begin{pmatrix} V_1 \\ I_1 \end{pmatrix} = \begin{pmatrix} a_{11} & a_{12} \\ a_{21} & a_{22} \end{pmatrix} \begin{pmatrix} V_2 \\ -I_2 \end{pmatrix} \tag{1}$$

where V_1 and I_1 are the input port voltage and current while V_2 and I_2 are the output port voltage and current respectively. Throughout this work we define the voltage gain as $A_v = (V_o/V_s)|_{I_o \to 0}$, the current gain as $A_i = (I_o/I_i)|_{V_o \to 0}$, the input impedance as $R_i = (V_s/I_i)|_{I_o \to 0}$ and the output impedance as $R_o = (V_o/I_o)|_{V_s \to 0}$.

2.1. Common-A amplifier topology

The common-A amplifier topology is shown in Figure 1(b) where a voltage source V_s with internal resistance R_s is connected to the input port of a two-port network representing an active device while the output port is loaded with an impedance R_L. Noting that $I_L = V_o/R_L$, the general expressions given in Table I may be derived for this configuration. The simplified expressions as $R_s \to 0$ are also given. For demonstration, we show how A_v was derived. In particular, it is clear from Figure 1(b) that $I_1 = I_i$ and that $V_2 = V_o|_{I_o \to 0}$. Hence, $A_v = V_o/V_s = V_2/(V_1 + I_1 R_s) = V_2/[a_{11}V_2 - a_{12}I_2 + (a_{21}V_2 - a_{21}I_2)R_s]$. Noting further that $I_2 = -V_2/R_L$ yields A_v as given in the first row of Table I.

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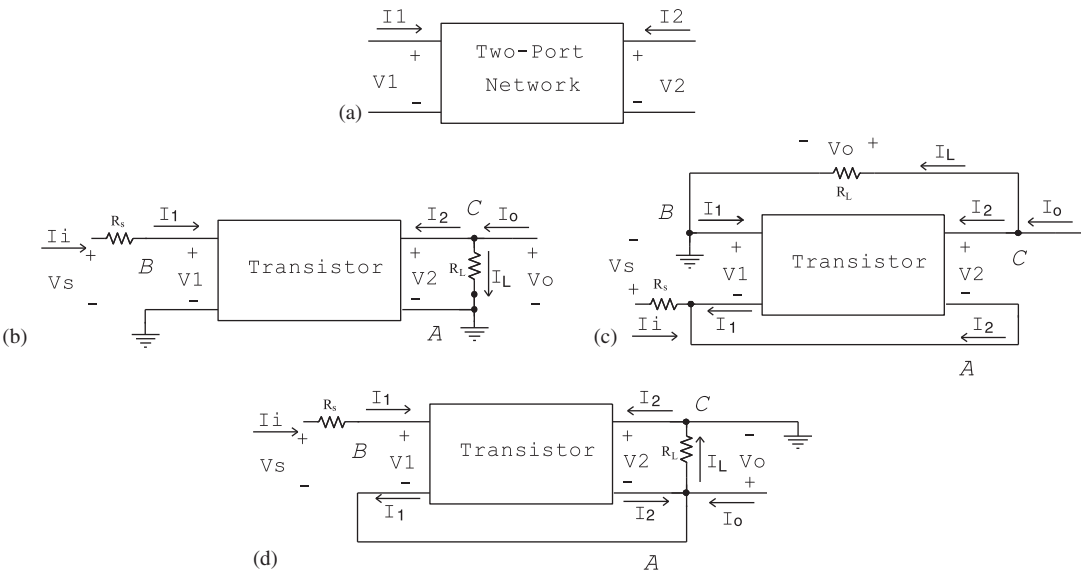

Figure 1. (a) Two-port network variables; (b) structure of common-A amplifier topology; (c) structure of common-B topology; and (d) structure of common-C topology.

Table I. Derived expressions for the Common-A amplifier.

	General expression	if $R_s \to 0$
A_v	$\left[a_{11}+\frac{a_{12}}{R_L}+\left(a_{21}+\frac{a_{22}}{R_L}\right)R_s\right]^{-1}$	$\left[a_{11}+\frac{a_{12}}{R_L}\right]^{-1}$
R_i	$\left[\left(a_{21}+\frac{a_{22}}{R_L}\right)A_v\right]^{-1}$	$\frac{a_{11}R_L+a_{12}}{a_{21}R_L+a_{22}}$
R_o	$\dfrac{a_{12}+a_{22}R_s}{a_{11}+\dfrac{a_{12}+a_{22}R_s}{R_L}+a_{21}R_s}$	$\dfrac{a_{12}}{a_{11}+\dfrac{a_{12}}{R_L}}$
A_i	$\frac{-1}{a_{22}}$	$\frac{-1}{a_{22}}$

2.2. *Common-B amplifier topology*

The common-B amplifier configuration is shown in Figure 1(c). Note in this case that there is a current feedback from the output port to the input port of the active device. Table II summarizes the derived expressions for this topology.

2.3. *Common-C amplifier topology*

The common-C amplifier configuration is shown in Figure 1(d). This structure is characterized by the expressions in Table III. Note that this topology has current feedforward from input port to

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Table II. Derived expressions for the Common-B amplifier.

	General expression	if $R_s \to 0$
A_v	$\dfrac{(a_{11}-1)(1+a_{21}R_s)+a_{21}(1-a_{11})R_s}{\left(a_{11}+\dfrac{a_{12}}{R_L}\right)(1+a_{21}R_s)+(1-a_{11})\left(a_{21}+\dfrac{a_{22}-1}{R_L}\right)R_s}$	$\dfrac{a_{11}-1}{a_{11}+\dfrac{a_{12}}{R_L}}$
R_i	$\dfrac{1+a_{21}R_s}{a_{21}-\left(a_{21}+\dfrac{a_{22}-1}{R_L}\right)A_v}$	$\left[a_{21}-\left(a_{21}+\frac{a_{22}-1}{R_L}\right)A_v\right]^{-1}$
R_o	$A_v\dfrac{R_s(1-a_{11})(a_{22}-1)+a_{12}(1+a_{21}R_s)}{(a_{11}-1)(1+a_{21}R_s)+a_{21}(1-a_{11})R_s}$	$A_v\dfrac{a_{12}}{a_{11}-1}$
A_i	$\dfrac{1}{a_{22}-1}$	$\dfrac{1}{a_{22}-1}$

Table III. Derived expressions for the common-C amplifier.

	General expression	if $R_s \to 0$
A_v	$\left[1-a_{11}-\dfrac{a_{12}}{R_L}+\dfrac{(R_s+a_{12})\left(a_{21}+\dfrac{a_{22}}{R_L}\right)}{a_{22}-1}\right]^{-1}$	$\left[1-a_{11}-\dfrac{a_{12}}{R_L}+\dfrac{a_{12}\left(a_{21}+\dfrac{a_{22}}{R_L}\right)}{a_{22}-1}\right]^{-1}$
R_i	$R_s+a_{12}+\dfrac{(a_{22}-1)\left(1-a_{11}-\dfrac{a_{12}}{R_L}\right)}{a_{21}+\dfrac{a_{22}}{R_L}}$	$a_{12}+\dfrac{(a_{22}-1)\left(1-a_{11}-\dfrac{a_{12}}{R_L}\right)}{a_{21}+\dfrac{a_{22}}{R_L}}$
R_o	$\dfrac{a_{12}(1-a_{22})+a_{22}(R_s+a_{12})}{\left(a_{11}-1+\dfrac{a_{12}}{R_L}\right)(1-a_{22})+\left(a_{21}+\dfrac{a_{22}}{R_L}\right)(R_s+a_{12})}$	$\left[\left(\frac{a_{11}-1}{a_{12}}+\frac{1}{R_L}\right)(1-a_{22})+\left(a_{21}+\frac{a_{22}}{R_L}\right)\right]^{-1}$
A_i	$\dfrac{1-a_{22}}{a_{22}}$	$\dfrac{1-a_{22}}{a_{22}}$

Table IV. Different two-port variable settings for the common-A, B and C amplifier topologies.

	V_1	V_2	I_1	I_2
Common-A	$V_s-I_iR_s$	V_o	I_i	$-(I_L-I_o)$
Common-B	$-(V_s-I_iR_s)$	$V_o-(V_s-I_iR_s)$	$(I_L-I_o)-I_i$	$-(I_L-I_o)$
Common-C	$(V_s-I_iR_s)-V_o$	$-V_o$	I_i	$(I_L-I_o)-I_i$

output port and has one terminal of the output port grounded. It is noted from all three tables that A_i is always independent of R_s and R_L.

In Table IV, the difference in two-port network variables ($V_{1,2}$ and $I_{1,2}$) between the three amplifier topologies is listed. Unlike traditional two-port analysis methods, we emphasize here that *the transmission matrix parameters of the core active element remain unchanged while the change is confined to the input and output variables*. In particular, the relationship of the four variables $V_{1,2}$ and $I_{1,2}$ to the physical variables V_s, V_o, I_i, I_o, I_L and R_s defines each specific topology.

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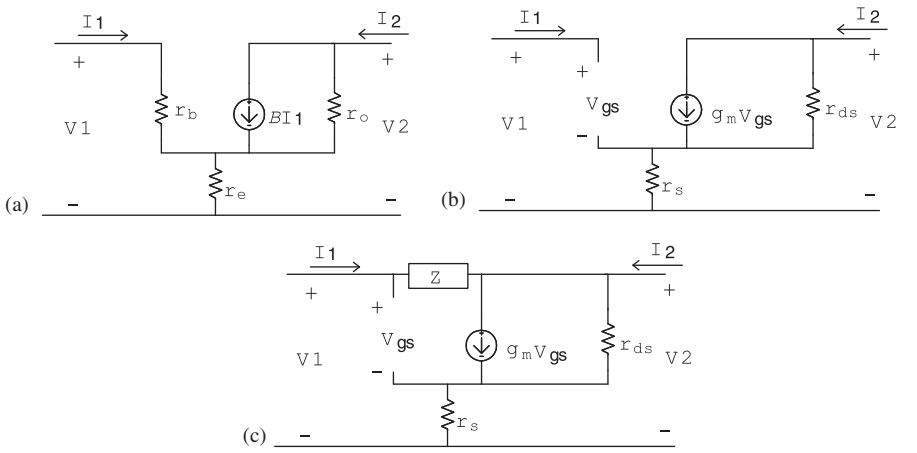

Figure 2. Simplified small signal equivalent circuits of: (a) BJT transistor; (b) MOS transistor; and (c) MOS transistor with gate-to-drain impedance Z.

3. APPLICATIONS OF THE PROPOSED TECHNIQUE

3.1. Single-stage BJT and MOS amplifiers

Figure 2(a) shows the small signal equivalent circuit of an NPN BJT transistor operating in the forward active mode. The model comprises two terminal resistors (r_b, r_e) and a dependent current-controlled current source βI_1 with output resistance r_o. β is the forward active current gain (assumed constant) and r_b is related to the BJT small-signal transconductance g_m as $r_b = \beta/g_\mathrm{m}$. It can be shown that the $[a]$ matrix for this equivalent circuit is

$$\begin{pmatrix} a_{11} & a_{12} \\ a_{21} & a_{22} \end{pmatrix} = \frac{-1}{\beta r_o - r_e} \begin{pmatrix} r_b + r_e & \beta r_e r_o + r_b(r_o + r_e) \\ 1 & r_o + r_e \end{pmatrix} \tag{2}$$

The above $[a]$ may be simplified if the assumptions $\beta r_o \gg r_e$ and $(1/\beta r_o) \to 0$ hold and then becomes

$$\begin{pmatrix} a_{11} & a_{12} \\ a_{21} & a_{22} \end{pmatrix} = \begin{pmatrix} \dfrac{-1}{g_\mathrm{m} r_o} & -\left(r_e + \dfrac{1}{g_\mathrm{m}} + \dfrac{r_e}{g_\mathrm{m} r_o}\right) \\ 0 & \dfrac{-1}{\beta} \end{pmatrix} = \begin{pmatrix} \dfrac{-1}{A} & -\left[r_e\left(1 + \dfrac{1}{A}\right) + \dfrac{1}{g_\mathrm{m}}\right] \\ 0 & \dfrac{-1}{\beta} \end{pmatrix} \tag{3}$$

where $A = g_\mathrm{m} r_o$. If A is sufficiently large such that $(1/A) \to 0$, a further simplification yields

$$\begin{pmatrix} a_{11} & a_{12} \\ a_{21} & a_{22} \end{pmatrix} = -\begin{pmatrix} 0 & r_e + \dfrac{1}{g_\mathrm{m}} \\ 0 & \dfrac{1}{\beta} \end{pmatrix} \tag{4}$$

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Table V. Application of the derived general expressions to BJT-based amplifiers.

	C-E	C-B	C-C
A_v	$-R_{\mathrm{L}}\Big/\left(r_e+\frac{1}{g_{\mathrm{m}}}\right)=-g_{\mathrm{m}}R_{\mathrm{L}}\mid_{r_e=0}$	$\frac{R_{\mathrm{L}}}{r_e+\frac{1}{g_{\mathrm{m}}}}=g_{\mathrm{m}}R_{\mathrm{L}}\mid_{r_e=0}$	$\left[1+\frac{r_e+1/g_{\mathrm{m}}}{R_{\mathrm{L}}}\right]^{-1}=1\mid_{R_{\mathrm{L}}\to\infty}$
R_i	$\beta\left(r_e+\frac{1}{g_{\mathrm{m}}}\right)=\beta/g_{\mathrm{m}}\mid_{r_e=0}$	$\frac{r_e+\frac{1}{g_{\mathrm{m}}}}{1+1/\beta}\approx\frac{1}{g_{\mathrm{m}}}\mid_{r_e=0}$	$\beta\left(R_{\mathrm{L}}+r_e+\frac{1}{g_{\mathrm{m}}}\right)$
R_o	R_{L}	R_{L}	$\left[\frac{1}{r_e+1/g_{\mathrm{m}}}+\frac{1}{R_{\mathrm{L}}}\right]^{-1}$ $=\left(r_e+\frac{1}{g_{\mathrm{m}}}\right)\mid_{R_{\mathrm{L}}\to\infty}$
A_i	β	$\frac{-1}{1+1/\beta}\approx-1$	$-\frac{1+1/\beta}{1/\beta}\approx-\beta$

Substituting the above matrix parameters in Tables I–III results in the widely known expressions for the common-emitter (C-E), common-base (C-B) and common-collector (C-C) BJT amplifier topologies, respectively, as given in Table V.

In a similar manner, and recalling the small signal equivalent circuit of an MOS transistor operating in the saturation mode (Figure 2(b)), it can be shown that the $[a]$ matrix for this circuit is

$$\begin{pmatrix} a_{11} & a_{12} \\ a_{21} & a_{22} \end{pmatrix}=\frac{-1}{g_{\mathrm{m}}r_{\mathrm{ds}}}\begin{pmatrix} 1 & r_s(1+g_{\mathrm{m}}r_{\mathrm{ds}})+r_{\mathrm{ds}} \\ 0 & 0 \end{pmatrix}\approx\begin{pmatrix} \dfrac{-1}{g_{\mathrm{m}}r_{\mathrm{ds}}} & -\left(r_s+\dfrac{1}{g_{\mathrm{m}}}\right) \\ 0 & 0 \end{pmatrix} \tag{5}$$

where g_{m} is the small signal transconductance, r_{ds} is the drain to source resistance (similar to r_o in the BJT) and r_s is the source resistance (similar to r_e in the BJT). Substituting in Tables I–III yields the well-known expressions for the common-source (C-S), common-gate (C-G) and common-drain (C-D) MOS amplifiers as given in Table VI.

It is worth noting that the modified transmission parameters that include parasitic effects, such as internal parasitic capacitors, or internal noise sources can also be derived and used for direct substitution in Tables I–III. Consider for example an MOS equivalent circuit that includes an impedance Z from gate to drain (typically a parasitic capacitor C_{gd}) (see Figure 2(c)). The MOS transmission matrix representation in this case is

$$\begin{pmatrix} a_{11} & a_{12} \\ a_{21} & a_{22} \end{pmatrix}=\frac{1}{r_{\mathrm{ds}}(1-g_{\mathrm{m}}Z)+r_s}\begin{pmatrix} r_{\mathrm{ds}}(1+g_{\mathrm{m}}r_s)+Z & r_{\mathrm{ds}}(1+g_{\mathrm{m}}r_s)Z \\ 1+g_{\mathrm{m}}r_{\mathrm{ds}} & r_{\mathrm{ds}}(1+g_{\mathrm{m}}r_s) \end{pmatrix} \tag{6}$$

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Table VI. Application of the derived general expressions to MOS-based amplifiers.

	C-S	C-G	C-D
A_v	$\left[\dfrac{-1}{g_m r_{ds}} - \dfrac{r_s+\dfrac{1}{g_m}}{R_L}\right]^{-1} = -g_m R_L\big\|_{r_s=0,\,r_{ds}=\infty}$	$\dfrac{\dfrac{1}{g_m r_{ds}}+1}{\dfrac{1}{r_s+\dfrac{1}{g_m}}} = g_m R_L\big\|_{r_s=0,\,r_{ds}=\infty}$	$\left[1+\dfrac{1}{g_m r_{ds}}+\dfrac{r_s+\dfrac{1}{g_m}}{R_L}\right]^{-1} = \dfrac{1g_m R_L}{1+g_m R_L}\Big\|_{r_s=0,\,r_{ds}=\infty} \approx 1$
R_i	∞	R_L/A_v	∞
R_o	$\dfrac{r_s+\dfrac{1}{g_m}}{\dfrac{1}{g_m r_{ds}}+\dfrac{r_s+\dfrac{1}{g_m}}{R_L}} = R_L\big\|_{r_{ds}=\infty}$	$A_v\dfrac{r_s+\dfrac{1}{g_m}}{\dfrac{1}{g_m r_{ds}}+1} = R_L\big\|_{r_s=0,\,r_{ds}=\infty}$	$\left(\dfrac{\dfrac{1}{g_m r_{ds}}+1}{r_s+\dfrac{1}{g_m}}+\dfrac{1}{R_L}\right)^{-1} = \dfrac{1}{g_m+\dfrac{1}{R_L}}\Big\|_{r_s=0,\,r_{ds}=\infty}$
A_i	∞	-1	∞

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Using the above matrix to evaluate the frequency response of the gain A_v for a common-A amplifier topology and by direct substitution in Table I assuming $R_s \to 0$ yields

$$A_v = \left(a_{11} + \frac{a_{12}}{R_L}\right)^{-1} = \frac{1 - \dfrac{g_m r_s}{1+g_m r_s} - \dfrac{g_m Z}{1+g_m r_s} + \dfrac{r_s}{r_{ds}(1+g_m r_s)}}{1 + \left(\dfrac{1}{r_{ds}(1+g_m r_s)} + \dfrac{1}{R_L}\right) Z} \tag{7}$$

since

$$\frac{g_m r_s}{1+g_m r_s} \approx 1, \quad \frac{r_s}{r_{ds}(1+g_m r_s)} \ll 1$$

and $r_{ds}(1+g_m r_s) \gg R_L$ are commonly valid assumptions, and for $Z = 1/sC_{gd}$ the above gain expression then simplifies to

$$A_v = \left(\frac{-g_m R_L}{1+g_m r_s}\right) \frac{1}{1+sC_{gd}R_L} \tag{8}$$

which as expected indicates a single pole frequency located at $1/C_{gd}R_L$ while the DC gain is still $-g_m R_L/(1+g_m r_s)$. Note that if we do not wish to make any assumptions or simplifications, the expression of (7) yields the more accurate A_v. We may obtain an even more accurate expression which includes R_s also by direct substitution in Table I; first column.

It is thus clear that more complicated transistor models do not imply re-analyzing any amplifier topology but simply require re-substitution in the derived expressions with a new transmission matrix corresponding to the new transistor model. This can be done with an analytically derived $[a]$ matrix, a numerically computed one or an experimentally measured one.

3.2. Differential amplifiers

A differential amplifier with equal load resistors R_L is shown in Figure 3(a). This structure is based on two common-A amplifiers. Assuming that the two employed transistors are matched implies having a similar transmission matrix. In the case that the resistance labelled R_E (see Figure 3(a)) does not exist, it is easy to show that the differential gain of this amplifier is $A_{vd} = (V_{o2} - V_{o1})/(V_2 - V_1) = R_L/a_{12}$ while the differential input resistance is $R_{id} = (V_2 - V_1)/(I_3 - I_1) = a_{12}/a_{22}$. Using the BJT transistor matrix (4) for example yields $A_{vd} = -R_L/(r_e + 1/g_m)$ and $R_{id} = \beta(r_e + 1/g_m)$; both expressions are similar to the C-E amplifier (Table V) as expected.

If the resistance R_E (see Figure 3(a)) exists, we obtain the general expressions

$$A_{vd} = \left(a_{11} + \frac{a_{12}}{R_L}\right)^{-1} \quad \text{and} \quad R_{id} = \frac{a_{12}}{a_{22}} + \frac{a_{11} - (a_{12}a_{21}/a_{22})}{a_{21} + (a_{22}/R_L)} \tag{9}$$

Note that A_{vd} and R_{id} are independent of R_E which may therefore be replaced with an ideal current source, as well known.

If the two transistors used in Figure 3(a) are not identical, we may assume that one of them is described by a set of transmission parameters $a_{11} \to a_{22}$ while the other is described by another set of parameters $b_{11} \to b_{22}$. After tedious calculations it can be shown in this case that

$$A_{vd} = \frac{b_{22}}{a_{22}\left(\dfrac{a_{21}}{b_{21}} - 1\right)\left(b_{11} + \dfrac{b_{11} - a_{11} + b_{12}}{R_L}\right)} \tag{10}$$

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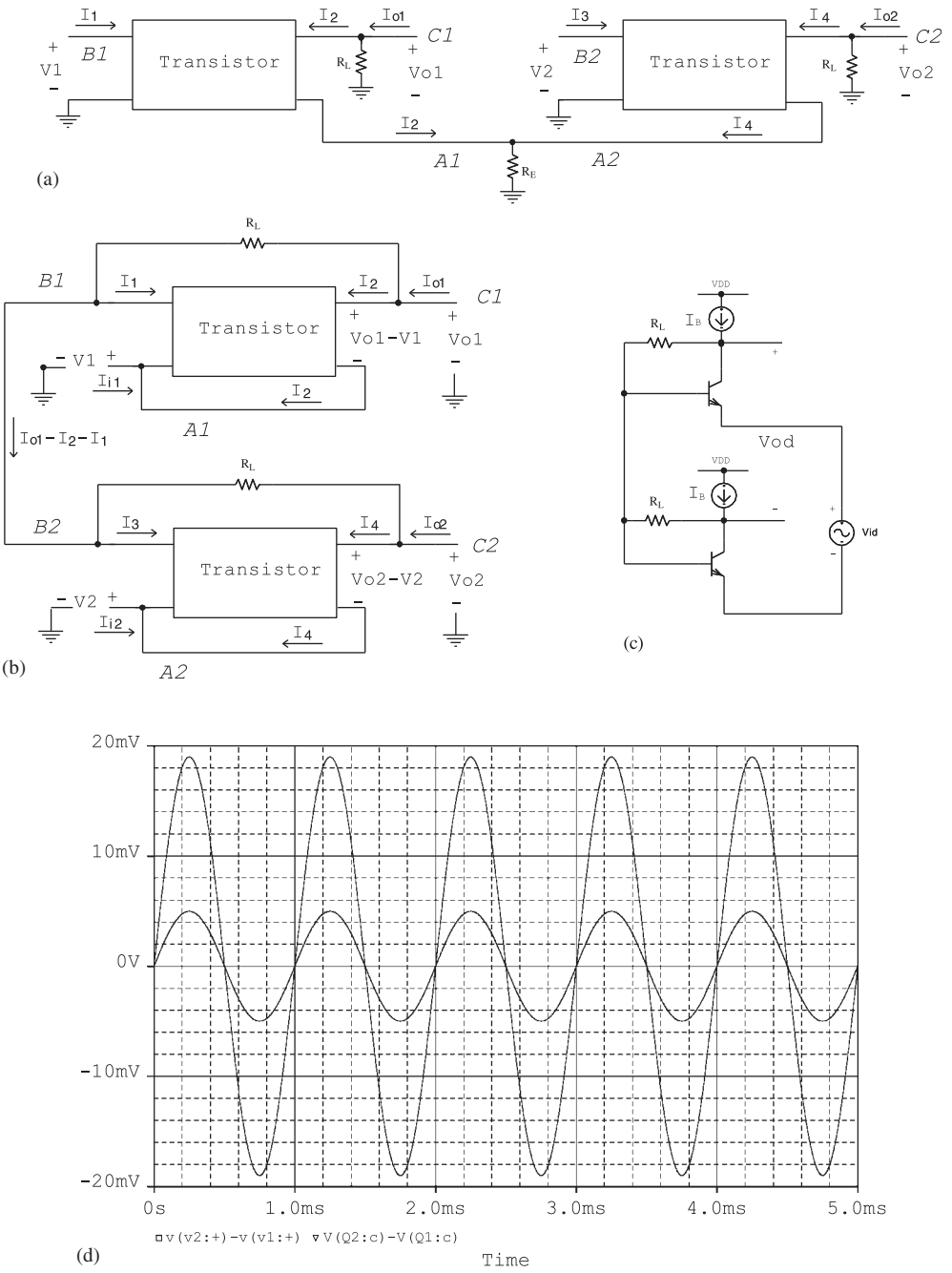

Figure 3. Differential amplifier structures: (a) conventional differential amplifier; (b) novel differential amplifier structure; (c) its circuit implementation; and (d) spice simulation of this novel structure ($V_{DD}=5\,\mathrm{V}$, $I_B=0.1\,\mathrm{mA}$, $R_\mathrm{L}=0.1\,\mathrm{k\Omega}$).

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which if using (4) reduces to $A_{\mathrm{vd}} = -(b_{22}/a_{22}b_{12})R_{\mathrm{L}} = (a_{22}/b_{22}a_{12})R_{\mathrm{L}}$. Despite the tedious calculations, this technique offers a straightforward method to evaluate the performance of a differential amplifier in the case that it is designed using different transistor types or if the transistors are not well matched.

As two-port representations offer a higher-level design insight, a novel alternative differential amplifier structure is proposed in Figure 3(b). This structure is based on two common-B amplifiers instead of Common-A amplifiers. Assuming that the two transistors have identical transmission parameters, this structure is described by

$$\begin{pmatrix} V_{\mathrm{o1}} - (I_{o1} - I_2)R_{\mathrm{L}} - V_1 \\ I_1 \end{pmatrix} = \begin{pmatrix} a_{11} & a_{12} \\ a_{21} & a_{22} \end{pmatrix} \begin{pmatrix} V_{\mathrm{o1}} - V_1 \\ -I_2 \end{pmatrix} \tag{11a}$$

and

$$\begin{pmatrix} V_{\mathrm{o2}} - (I_{o2} - I_4)R_{\mathrm{L}} - V_2 \\ I_3 \end{pmatrix} = \begin{pmatrix} a_{11} & a_{12} \\ a_{21} & a_{22} \end{pmatrix} \begin{pmatrix} V_{\mathrm{o2}} - V_2 \\ -I_4 \end{pmatrix} \tag{11b}$$

It can then be shown using (4) that the differential gain is $A_{\mathrm{vd}} = -R_{\mathrm{L}}/a_{12} = R_{\mathrm{L}}/(r_e + 1/g_{\mathrm{m}})$. Figure 3(c) shows a BJT circuit implementation of this differential amplifier. Spice simulation using Q2N2222 BJT transistors biased to have $g_{\mathrm{m}} = 38\,\mathrm{mA/V}$ ($A_v \approx g_{\mathrm{m}}R_{\mathrm{L}} = 3.8$) is shown in Figure 3(d).

3.3. Multiple-stage amplifiers

Multi-stage amplifiers are commonly used in many applications. In this section, we analyze the demonstrative example of a two-stage common-A–common-C amplifier, as shown in Figure 4. The two-stage amplifier is described by

$$\begin{pmatrix} V_{\mathrm{s}} - I_i R_{\mathrm{s}} \\ I_i \end{pmatrix} = \begin{pmatrix} a_{11} & a_{12} \\ a_{21} & a_{22} \end{pmatrix} \begin{pmatrix} V_2 \\ I_3 + \dfrac{V_2}{R} \end{pmatrix} \quad \text{and} \quad \begin{pmatrix} V_2 - V_O \\ I_3 \end{pmatrix} = \begin{pmatrix} b_{11} & b_{12} \\ b_{21} & b_{22} \end{pmatrix} \begin{pmatrix} -V_O \\ I_3 + I_O - \dfrac{V_O}{R_{\mathrm{L}}} \end{pmatrix} \tag{12}$$

where $a_{11} \to a_{22}$ and $b_{11} \to b_{22}$ are two-port transmission parameters for the two transistors used If we assume for simplicity two similar transistors with the same transmission parameters, it can then be shown that the total two-stage gain $A_v|_{I_o \to 0}$ and input resistance $R_i|_{I_o \to 0}$ at $R_{\mathrm{s}} = 0$ are

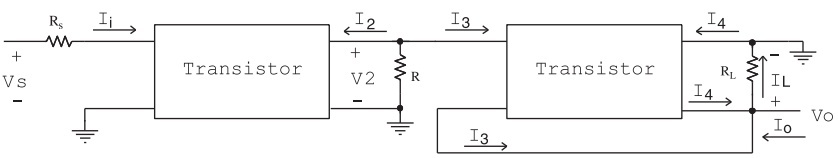

Figure 4. Two-stage common-A–common-C amplifier.

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given, respectively, by

$$A_v = \left[\left(1+a_{11}+\frac{a_{12}}{R}\right) \frac{a_{12}\left(a_{21}+\dfrac{a_{22}}{R_\mathrm{L}}\right)}{(a_{22}-1)} + \left(a_{11}+\frac{a_{12}}{R}\right)\left(1-a_{11}-\frac{a_{12}}{R_\mathrm{L}}\right) \right]^{-1} \tag{13a}$$

$$R_i = \frac{1}{A_v}\left[\left(a_{21}+\frac{a_{22}}{R}\right)\left(1-a_{11}-\frac{a_{12}}{R_\mathrm{L}}\right) + \frac{\left(a_{21}+\frac{a_{22}}{R_\mathrm{L}}\right)\left(a_{22}+a_{12}\left(a_{21}+\frac{a_{22}}{R}\right)\right)}{(a_{22}-1)} \right]^{-1} \tag{13b}$$

using (4) for BJT transistors and substituting in the above equations yields

$$A_v = -\left[\frac{r_e+1/g_\mathrm{m}}{(\beta+1)R_\mathrm{L}}\left(1-\frac{r_e+1/g_\mathrm{m}}{R}\right) + \frac{r_e+1/g_\mathrm{m}}{R}\left(1+\frac{r_e+1/g_\mathrm{m}}{R_\mathrm{L}}\right) \right]^{-1} \tag{14a}$$

$$R_i = \frac{-1}{A_v}\left[\frac{1}{\beta R}\left(1+\frac{r_e+1/g_\mathrm{m}}{R_\mathrm{L}}\right) + \frac{1-\dfrac{r_e+1/g_\mathrm{m}}{R}}{\beta R_\mathrm{L}(\beta+1)} \right]^{-1} \tag{14b}$$

At $R_\mathrm{L}\to\infty$, $A_v = -R/(r_e+1/g_\mathrm{m}) \approx -g_\mathrm{m}R$, which is the gain of the common-A stage only, as expected, since the common-C stage is a voltage buffer (recall Table V). Also $R_\mathrm{L}\to\infty$ yields $R_i = \beta/(r_e+1/g_\mathrm{m})$, which is the input resistance of the common-A stage only.

3.4. Other application circuits

We demonstrate here three more non-amplifier analysis applications. Consider the cross-coupled transistor pair of Figure 5(a) and its two-port model. Here, we illustrate the method assuming that BJT transistors are used. Using (4) and assuming two similar transistors, it can be easily shown that $V_1 - V_2 = V^+ - V^- = a_{12}(I_4 - I_2)$. Also $I^+ - I^- = (1+a_{22})(I_4 - I_2)$ resulting in negative differential input resistance

$$R_i = \frac{V^+ - V^-}{I^+ - I^-} = \frac{a_{12}}{1+a_{22}} = \frac{-(r_e+1/g_\mathrm{m})}{1-1/\beta} \approx -(r_e+1/g_\mathrm{m})$$

as is well known.

The second example of a simple current mirror is shown in Figure 5(b) which using (4) and assuming similar transmission parameters for the two transistors has $V_i = -a_{12}I_2 = -a_{12}I_o$ and $I_3 = -a_{22}I_o$. Hence, $I_i = I_1 + I_2 + I_3 = (1-2a_{22})I_o$ and the current transfer ratio $I_o/I_i = 1/(1-2a_{22}) = 1/(1+2/\beta) \approx 1$. The input resistance of the diode connected transistor is $V_i/I_i = -a_{12}/(1-2a_{22}) \approx r_e + 1/g_\mathrm{m}$.

One last example is shown in Figure 5(c) representing a Darlington pair composite transistor described using (4) by

$$\begin{pmatrix} V_i - V_c \\ I_i \end{pmatrix} = \begin{pmatrix} 0 & a_{12} \\ 0 & a_{22} \end{pmatrix} \begin{pmatrix} -V_2 \\ -I_2 \end{pmatrix} \quad \text{and} \quad \begin{pmatrix} -V_2 - V_c \\ I_2 \end{pmatrix} = \begin{pmatrix} 0 & a_{12} \\ 0 & a_{22} \end{pmatrix} \begin{pmatrix} V_\mathrm{o} - V_c \\ -I_o \end{pmatrix} \tag{15}$$

assuming identical transistors. It is thus seen that $I_o = I_i/a_{22}^2 = \beta^2 I_i$ (with a very high current gain as expected) and $R_i|_{V_c=0} = V_i/I_i = a_{12}/a_{22} = \beta(r_e + 1/g_\mathrm{m})$.

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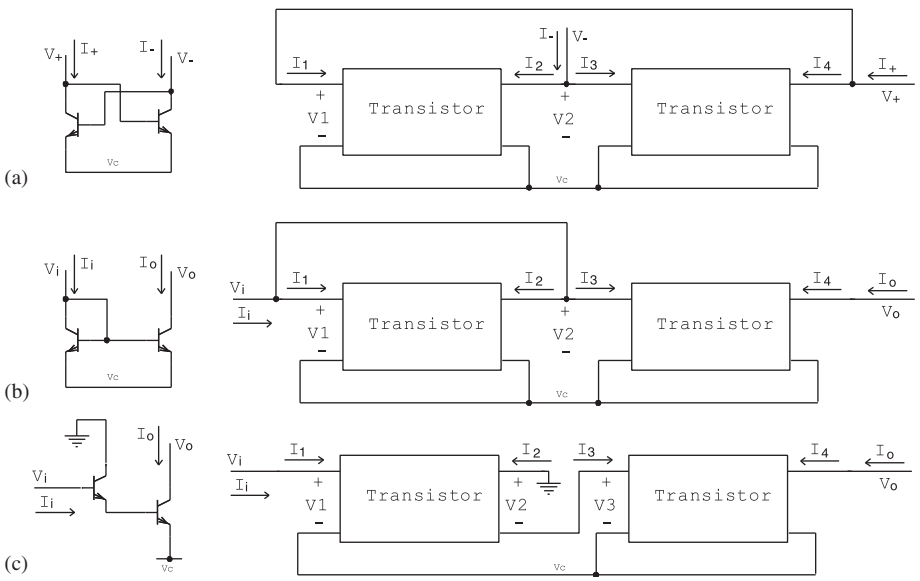

Figure 5. Two-port representations of: (a) cross-coupled transistor pair; (b) current mirror; and (c) Darlington pair.

These three examples clearly show the value of the proposed analysis technique which in all cases maintains the $[a]$ matrix representative only of the active device (transistor) while the change in connectivity is mapped into a change into input and output two-port variables.

4. COMPOSITE CASCADES

The transmission matrix is particularly adopted to the cascade of two ports since it multiplies in the order of the cascade. As a feature of using transmission matrix representations, a few useful composite cascades can be derived. Consider for example an MOS-BJT cascade which using (4) and (5) will have the equivalent transmission matrix‡

$$\begin{pmatrix} \dfrac{1}{g_{\mathrm{mm}} r_{\mathrm{ds}}} & r_s + \dfrac{1}{g_{\mathrm{mm}}} \\ 0 & 0 \end{pmatrix} \begin{pmatrix} 0 & r_e + \dfrac{1}{g_{mb}} \\ 0 & \dfrac{1}{\beta} \end{pmatrix} = \begin{pmatrix} 0 & \dfrac{r_e + \dfrac{1}{g_{mb}}}{g_{\mathrm{mm}} r_{\mathrm{ds}}} + \dfrac{r_s + \dfrac{1}{g_{\mathrm{mm}}}}{\beta} \\ 0 & 0 \end{pmatrix} \tag{16}$$

where g_{mm} and g_{mb} are respectively the MOS and BJT transconductances. However, a BJT-MOS cascade will yield a transmission matrix with all zero coefficients, as expected, since in such a cascade the two transistors are off due to the zero MOS gate current. A few other composites are given in Table VII and illustrated in Figure 6.

‡Recall that two networks $[a_1]$ and $[a_2]$ in cascade have the equivalent transmission matrix $[a_{12}] = [a_1] \cdot [a_2]$.

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Table VII. Important composite transistor cascades (g_{mm} and g_{mb} are, respectively, the MOS and BJT transconductances).

Cascade	Equivalent matrix
Floating Z-MOS	
Figure 6(a)	$\begin{pmatrix} 1 & Z \\ 0 & 1 \end{pmatrix}\begin{pmatrix} \frac{1}{g_{\mathrm{mm}}r_{\mathrm{ds}}} & r_s+\frac{1}{g_{\mathrm{mm}}} \\ 0 & 0 \end{pmatrix}=\begin{pmatrix} \frac{1}{g_{\mathrm{mm}}r_{\mathrm{ds}}} & r_s+\frac{1}{g_{\mathrm{mm}}} \\ 0 & 0 \end{pmatrix}$
Grounded Z-MOS	
Figure 6(b)	$\begin{pmatrix} 1 & 0 \\ 1/Z & 1 \end{pmatrix}\begin{pmatrix} \frac{1}{g_{\mathrm{mm}}r_{\mathrm{ds}}} & r_s+\frac{1}{g_{\mathrm{mm}}} \\ 0 & 0 \end{pmatrix}=\begin{pmatrix} \frac{1}{g_{\mathrm{mm}}r_{\mathrm{ds}}} & r_s+\frac{1}{g_{\mathrm{mm}}} \\ \frac{1}{g_{\mathrm{mm}}r_{\mathrm{ds}}Z} & \frac{r_s+\frac{1}{g_{\mathrm{mm}}}}{Z} \end{pmatrix}$
Floating Z-BJT	
Figure 6(a)	$\begin{pmatrix} 1 & Z \\ 0 & 1 \end{pmatrix}\begin{pmatrix} 0 & r_e+\frac{1}{g_{mb}} \\ 0 & \frac{1}{\beta} \end{pmatrix}=\begin{pmatrix} 0 & r_e+\frac{1}{g_{mb}}+\frac{Z}{\beta} \\ 0 & \frac{1}{\beta} \end{pmatrix}$
Grounded Z-BJT	
Figure 6(b)	$\begin{pmatrix} 1 & 0 \\ 1/Z & 1 \end{pmatrix}\begin{pmatrix} 0 & r_e+\frac{1}{g_{mb}} \\ 0 & \frac{1}{\beta} \end{pmatrix}=\begin{pmatrix} 0 & r_e+\frac{1}{g_{mb}} \\ 0 & \frac{r_e+\frac{1}{g_{mb}}}{Z}+\frac{1}{\beta} \end{pmatrix}$
MOS-floating Z	
Figure 6(c)	$\begin{pmatrix} \frac{1}{g_{\mathrm{mm}}r_{\mathrm{ds}}} & r_s+\frac{1}{g_{\mathrm{mm}}} \\ 0 & 0 \end{pmatrix}\begin{pmatrix} 1 & Z \\ 0 & 1 \end{pmatrix}=\begin{pmatrix} \frac{1}{g_{\mathrm{mm}}r_{\mathrm{ds}}} & r_s+\frac{1}{g_{\mathrm{mm}}}+\frac{Z}{g_{\mathrm{mm}}r_{\mathrm{ds}}} \\ 0 & 0 \end{pmatrix}$
MOS-grounded Z	
Figure 6(d)	$\begin{pmatrix} \frac{1}{g_{\mathrm{mm}}r_{\mathrm{ds}}} & r_s+\frac{1}{g_{\mathrm{mm}}} \\ 0 & 0 \end{pmatrix}\begin{pmatrix} 1 & 0 \\ 1/Z & 1 \end{pmatrix}=\begin{pmatrix} \frac{1}{g_{\mathrm{mm}}r_{\mathrm{ds}}}+\frac{r_s+\frac{1}{g_{\mathrm{mm}}}}{Z} & r_s+\frac{1}{g_{\mathrm{mm}}} \\ 0 & 0 \end{pmatrix}$
BJT-floating Z	
Figure 6(c)	$\begin{pmatrix} 0 & r_e+\frac{1}{g_{mb}} \\ 0 & \frac{1}{\beta} \end{pmatrix}\begin{pmatrix} 1 & Z \\ 0 & 1 \end{pmatrix}=\begin{pmatrix} 0 & r_e+\frac{1}{g_{mb}} \\ 0 & \frac{1}{\beta} \end{pmatrix}$
BJT-grounded Z	
Figure 6(d)	$\begin{pmatrix} 0 & r_e+\frac{1}{g_{mb}} \\ 0 & \frac{1}{\beta} \end{pmatrix}\begin{pmatrix} 1 & 0 \\ 1/Z & 1 \end{pmatrix}=\begin{pmatrix} \frac{r_e+\frac{1}{g_{mb}}}{Z} & r_e+\frac{1}{g_{mb}} \\ \frac{1}{\beta Z} & \frac{1}{\beta} \end{pmatrix}$

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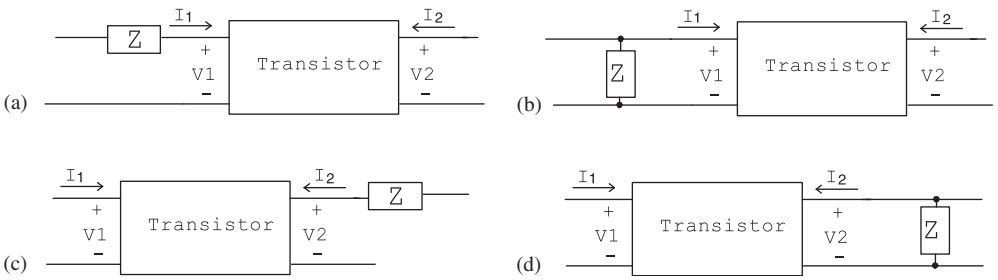

Figure 6. Some possible composite cascades.

5. CONCLUSION

We have presented here a simplified amplifier analysis technique using two-port transmission parameters. Of particular importance is the generic nature of the derived formulae, which can apply to both BJT or MOS amplifiers; each with its respective transmission matrix and indeed to any alternative active device. We have also applied the technique to non-amplifier circuits.

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