was measured in the frequency range 2.075 to 3.250 GHz (44% bandwidth). The large input impedance bandwidth was due to the tilted upper patch. This was confirmed by several experiments with patches of the same dimensions but both parallel to the ground plane. By varying the spacings between the patches, the largest obtained bandwidth was ~10%.

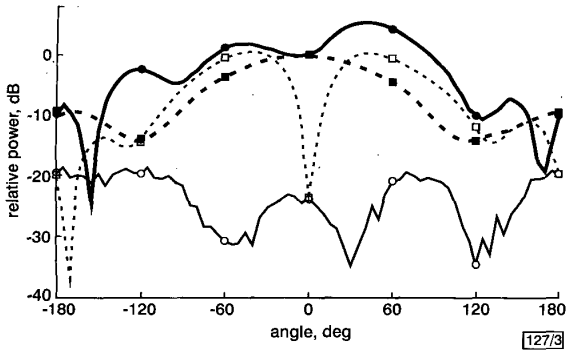

Fig. 3 *Measured radiation patterns at 2.0 GHz*
E-plane, co-polarisation
E-plane, cross-polarisation
H-plane, co-polarisation
H-plane, cross-polarisation

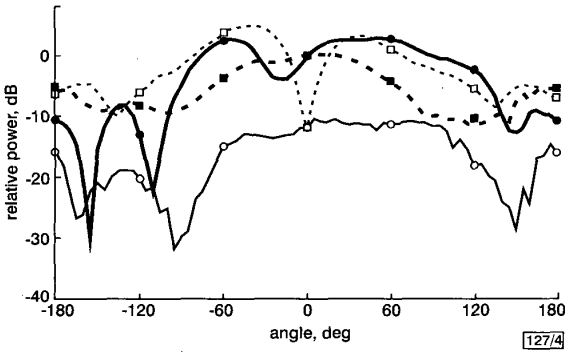

Fig. 4 *Measured radiation patterns at 2.6 GHz*
E-plane, co-polarisation
E-plane, cross-polarisation
H-plane, co-polarisation
H-plane, cross-polarisation

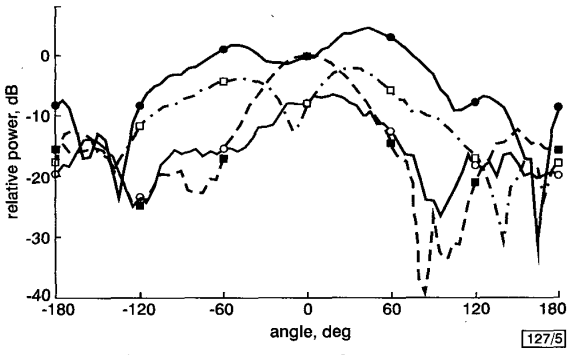

Fig. 5 *Measured radiation patterns at 3.2 GHz*
E-plane, co-polarisation
E-plane, cross-polarisation
H-plane, co-polarisation
H-plane, cross-polarisation

The measured co-polarisation and cross-polarisation radiation patterns in the E- and H-planes at 2.0, 2.6 and 3.2 GHz are shown in Figs. 3 – 5, respectively. All the patterns are normalised to the co-polarisation level in the direction of 0°. The co-polarisation maximum in the E-plane is shifted in the direction of about +45° and the pattern has a second lobe, 0.2–3.6 dB below maximum, at around –45°. The cross-polarisation levels in the H-plane are quite high. Similar behaviour of the cross-polarisation in the H-plane has been reported [5 – 7]. However, such high cross-polarisation levels in the H-plane should not be a disadvantage for mobile communications in urban environments with large amounts of scattering, diffraction and reflections. The gain of this antenna, measured in the E-plane beam maximum direction, is between 2 and 3 dBi in the whole bandwidth considered.

Conclusion: A novel compact patch antenna is presented. By using a stacked patch structure with a tilted parasitic (upper) patch, a wide input impedance bandwidth has been obtained. The radiation patterns in both the E- and H-planes do not significantly change in the bandwidth considered. A satisfactory gain has been measured in the direction of maximum radiation. These results indicate that the antenna can have an application in present and future mobile communication systems.

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Fractional-order Wien-bridge oscillator

W. Ahmad, R. El-khazali and A.S. Elwakil

The classical Wien-bridge sinusoidal oscillator is studied, when both of the capacitors of the oscillator acquire a fractional order. Accordingly, the Wien oscillator is described by a set of fractional-order nonlinear differential equations. It is shown that sinusoidal oscillations are preserved but the phase-shift between the waveforms of the two state variables and the frequency of oscillation both depend on the fractional-order, leading to a significant advantage over the integer-type Wien oscillator. Findings are validated via numerical simulations.

Introduction: There has been growing interest recently in studying fractional-order systems and electronic circuits [1 – 5]. Such systems are described by noninteger-order differential equations following the generalised form of calculus known as *fractional calculus* [7]. Despite speculation that a fractance energy-storage device might soon be commercially available [8], such a device is not yet available, therefore studies of fractional-order circuits have relied basically on a method where integer-order capacitors interconnected in geometrically-scaled networks simulate a single fractional-order device [2, 3]. The limitations of such a method are obvious and therefore constructing experimental setups for fractional-order circuits is still not feasible in practice. Regarding numerical simulation, there are generally two methods to simulate the behaviour of a fractional-order system. The first method is based on deriving a higher-order integer system which is approxi-

mately equivalent to the original fractional system [4]. The second method relies on integrating in the time domain the system equations [5, 6] using the gamma-function-based definitions of [7] for fractional derivatives.

In this Letter, we investigate the classical Wien-bridge oscillator when both of its capacitors are assumed fractional. By definition, a fractional capacitor is one where the current-voltage relation $(1/C)i_c = d^{\alpha}v_c/dt^{\alpha}$, with α not necessarily integer, holds.

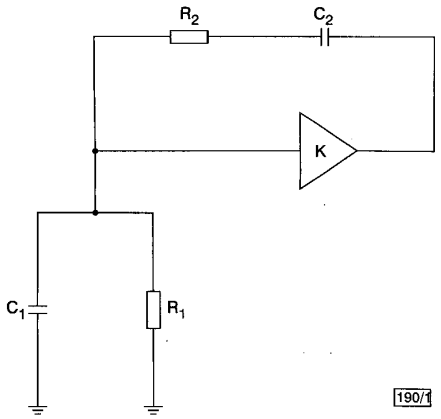

Fig. 1 *Classical Wien-bridge oscillator structure with noninverting amplifier*

Fractional-order Wien oscillator: Consider the Wien-bridge oscillator shown in Fig. 1 with two linear resistors and two fractional-order capacitors. For simplicity, we consider the case where $R_1 = R_2 = R$ and $C_1 = C_2 = C$. In general, the two capacitors might not be equal in value or in order. However, we assume here that both capacitors also have the same fractional order α.

By setting $X_1 = V_{C1}/V_{sat}$, $X_2 = V_{C2}/V_{sat}$, where V_{sat} is the saturation voltage of the noninverting amplifier (see Fig. 1), and by normalising time with respect to RC, the state-space representation of this oscillator is given by

$$D^{\alpha}\begin{pmatrix}X_1\\X_2\end{pmatrix} = \begin{pmatrix}a-2 & -1\\ a-1 & -1\end{pmatrix}\begin{pmatrix}X_1\\X_2\end{pmatrix} + \begin{pmatrix}b\\b\end{pmatrix} \qquad (1)$$

where

$$(a,b) = \begin{cases}(0,1) & KX_1 \geq 1\\ (K,0) & -1 < KX_1 < 1\\ (0,-1) & KX_1 \leq 1\end{cases}$$

and where K is the gain of the amplifier in its linear region and the operator $D\alpha \equiv d^{\alpha}/dt^{\alpha}$. Eqn. 1 represents a fractional-order differential equation with a saturation-type nonlinearity. Using the stability condition for fractional systems derived in [9], it can be shown that a pair of pure imaginary eigenvalues is created when $K = 3 + 2\cos(\alpha\pi/2)$. In this case, the frequency of oscillation ω_{α} is equal to $(RC)^{-1/\alpha}$. In the special case $\alpha = 1$, the well-known oscillation condition ($K = 3$) and frequency ($\omega_0 = 1/RC$) for the classical Wien oscillator are retrieved. Note that the frequency of oscillation can be changed by varying the fractional-order α without changing the capacitor value C. In particular, $\omega_{\alpha} = (\omega_0)^{1/\alpha}$; for $\alpha < 1$, it is clear that extended oscillation frequencies are feasible.

Numerical simulations of eqn. 1 were carried out using the backward difference method based on the Grünwald-Letnikov approximation of a fractional derivative [10] given by:

$$\frac{d^{\alpha}X}{dt^{\alpha}} \triangleq h^{-\alpha}\sum_{j=0}^{m}(-1)^j n_j^{\alpha} X(m-j) \qquad (2)$$

where h is the integration step. The waveforms of the two state variable X_1 and X_2 at four different values of α are shown, respectively, in Fig. 2. It can be noticed that the amplitude of the waveforms increases with α. Indeed, from eqn. 2 when $h \rightarrow 0$, the amplitude depends on the factor $n_j^{\alpha} = \alpha(\alpha-1)...(\alpha-j+1)/j$, which increases with α. From Fig. 2, it is also clear that the phase-shift between X_1 and X_2 increases with α. In Fig. 3*a*, variation of the phase-shift with α is plotted. The special case $\alpha = 1$ corresponds to $\pi/4$ phase-shift, as expected. This is shown by the change in frequency when α is changed, Fig. 3*b* shows the waveform of X_1 for $\alpha = 0.5$ and $\alpha = 1$, respectively, with $RC = 0.5$. It is clear that $\omega_{0.5} = 2\omega_1$ for the same RC.

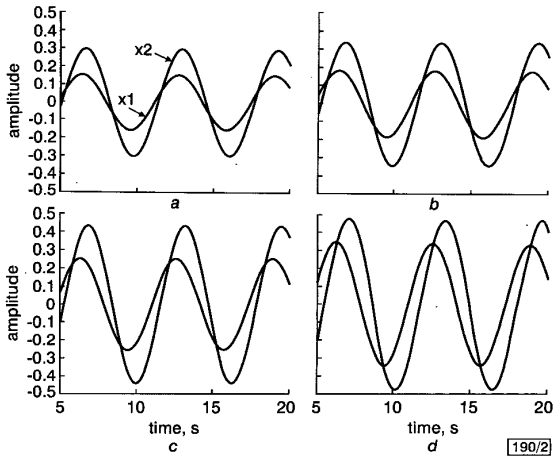

Fig. 2 *Numerical simulations of noninteger-order nonlinear differential eqn. 1*

a $\alpha = 0.3$ *b* $\alpha = 0.5$
c $\alpha = 0.7$ *d* $\alpha = 1.0$
Plots represent X_1 and X_2 state variables

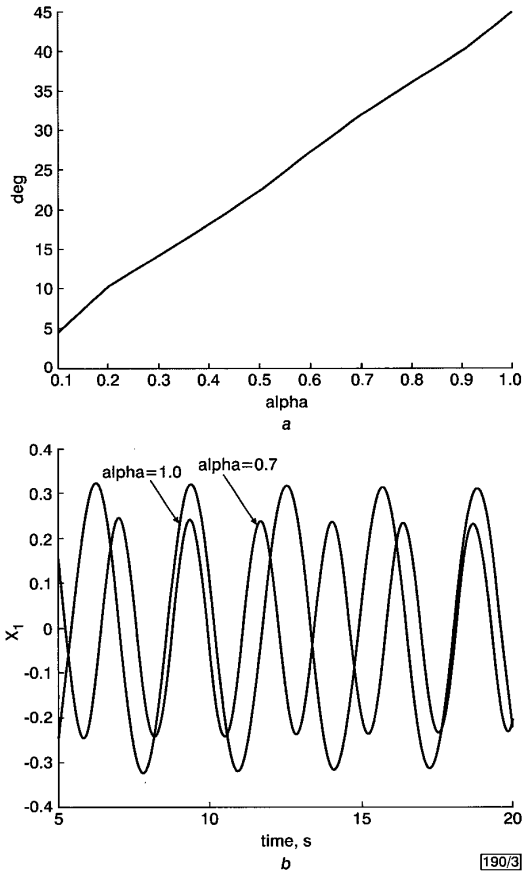

Fig. 3 *Phase-shift against fractional order α and variation of oscillation frequency against α*

a Phase-shift against α
b Oscillation frequency against α

Conclusion: We have verified that a fractional-order Wien-bridge oscillator with two equal-value equal-order capacitors can sustain sinusoidal oscillations. The condition and the frequency of oscillation are both functions of the noninteger order. A clear advantage of this fractional oscillator is the possibility of obtaining high frequencies by reducing the order of the capacitors rather than their value, which can remain sufficiently large. It is worth noting that attempts to fabricate fractal capacitors have already shown some success [8].

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Phase interpolation direct digital synthesiser with precise delay generator using two-step integration

H. Nosaka, Y. Yamaguchi and M. Muraguchi

A new delay generator using two-step integration is proposed for direct digital synthesis. The new delay generator can provide precise delay timing since delay timing is unaffected by the propagation delay dispersion of the voltage comparator. Experimental results show that the frequency synthesiser operated successfully.

Introduction: The fast frequency switching of frequency synthesisers has become an important requirement in advanced wireless communication systems. Fast frequency switching within the guard time allows channels to be assigned dynamically in time-division multiple-access (TDMA) systems. Fast switching also allows the use of the frequency-hopping spread-spectrum (FH-SS) technique, which performs better with respect to the near-far effect than the direct-sequence spread-spectrum (DS-SS) technique [1].

Direct digital synthesisers (DDSs) switch their output frequencies quickly because they have no feedback loop, unlike phase-locked-loop (PLL) frequency synthesisers. DDSs, however, consume a large amount of power. Phase-interpolation DDSs have been proposed in an attempt to realise a low-power DDS [2 – 4]. In this type of DDS, the purity of the output frequency is determined by the accuracy of the delay generator, which eliminates the timing jitter in the accumulator overflow pulses. In conventional delay generators, the propagation-delay dispersion of the voltage comparator generates timing jitter in the DDS output. In this Letter, we describe a new delay generator that uses two-step integration, and which eliminates the effect of dispersion on the delay timing.

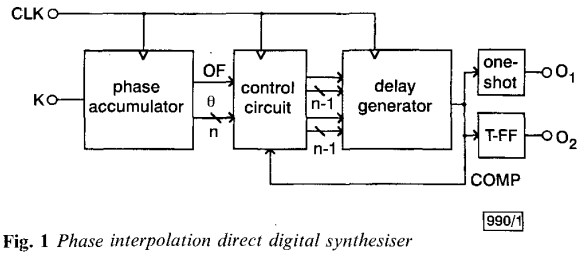

Fig. 1 *Phase interpolation direct digital synthesiser*

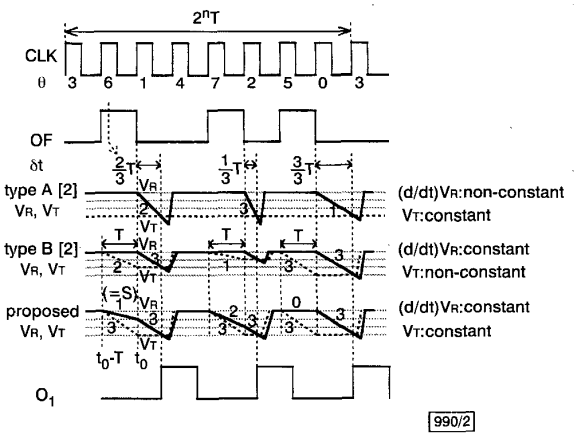

Fig. 2 *Comparison of phase interpolation techniques for direct digital synthesis*

Circuit configuration: A block diagram of the DDS is shown in Fig. 1. An n-bit phase accumulator with frequency control word K overflows K-times within a period of $2n{\cdot}T$ where T is one clock cycle. Thus, the fundamental frequency of the overflow signal (OF) is given by

$$f_{OF} = \frac{K}{2^n} f_{CLK} \tag{1}$$

where f_{CLK} is the clock frequency. The overflow signal, however, contains very high levels of spurious frequency components because the time intervals of the rising edges change periodically in a period of $2^n{\cdot}T$. The delay generator produces pulses the rising edges of which occur at a constant time interval. The delay time, δt, is given by

$$\delta t(\theta) = \frac{2^n - \theta}{K} T \tag{2}$$

where θ is the output data of the accumulator. The delay generator is the key circuit in the phase-interpolation DDS because the spurious performance is determined there. Fig. 2 compares the operation of three delay generators for $n = 3$ and $K = 3$. All the delay generators produce delay timing by means of the coincidence of ramp wave voltage, V_R, and threshold voltage, V_T. In conventional delay generators (type A [2] and type B [4]), either the slope of V_R, (d/dt) V_R, or V_T varies for different delay timing. This generates jitter when the voltage comparator used to detect the coincidence of V_R and V_T has a propagation delay dispersion caused by (d/dt) V_R or V_T. Furthermore, it is difficult to reduce the power consumption without degrading the dispersion. We propose a new delay generator using the two-step integration of V_R to solve these problems. Fig. 3 shows our proposed delay generator. The threshold voltage, V_T, is generated by the one-clock-cycle integration of K and by holding of the integrated voltage. The held voltage $(t_0 \le t)$ is given by

$$V_T = -\frac{KI_0}{C} T \tag{3}$$

The ramp wave, V_R, is produced by a one-clock-cycle integration of S $(t_0 - T \le t < t_0)$ and the following integration of K $(t_0 \le t)$,

$$V_R = -\frac{SI_0}{C} T - \frac{KI_0}{C}(t - t_0) \tag{4}$$