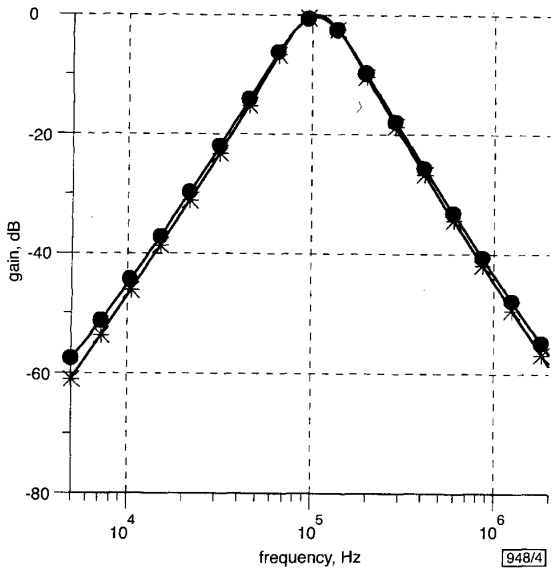

Fig. 4 *PSPICE simulation result using CMOS FTFN in Fig. 1 and ideal model*

—✳— ideal FTFN
—●— proposed FTFN

Conclusion: A new technology for the realisation of a CMOS FTFN has been presented. The proposed translinear CMOS FTFN circuit, which uses a translinear cell based architecture, provides an alternative solution to a differential amplifier-based FTFN circuit. PSPICE simulations shows that the proposed circuit provides high performance in terms of the frequency response and dynamic range as well as the other advantages of the translinear cell-based active elements. The feasibility of the circuit has been tested on a current-mode bandpass filter.

15 May 2000
Electronics Letters Online No: 20000927
DOI: 10.1049/el:20000927

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Low-voltage relaxation oscillator

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A relaxation oscillator employing an S-shaped current-controlled nonlinear resistor composed of two bipolar transistors and a single resistor is proposed. The oscillator produces a unipolar sawtooth waveform and is suitable for low-voltage applications.

Introduction: Relaxation oscillators produce signals which abruptly switch between at least two different states. This rapid regenerative switching manifests itself as hysteresis in these oscillators. The hysteresis phenomenon has been carefully studied in [1] where it was shown that static resistive models of hysteresis which assume discontinuous driving-point characteristics (jumps) are incorrect. In particular, hysteresis is a dynamic behaviour resulting from the existence of a parasitic capacitor or inductor associated with fundamentally nonlinear voltage or current-controlled driving-point characteristics. It is essential to consider these parasitics to model correctly a relaxation oscillator and reproduce its dynamics [1]. Since parasitic elements have infinitesimally small values (compared to similar elements in the circuit), relaxation oscillators exhibit slow-fast dynamics and are modelled by stiff systems of differential equations with a minimum order of two. Most relaxation oscillators in the literature rely on active nonlinear resistors [2 – 4]. However, this is not necessary and passive nonlinear resistors [5] suffice.

In this Letter, we describe a relaxation oscillator particularly suitable for low-voltage applications. There are no active elements in the circuit.

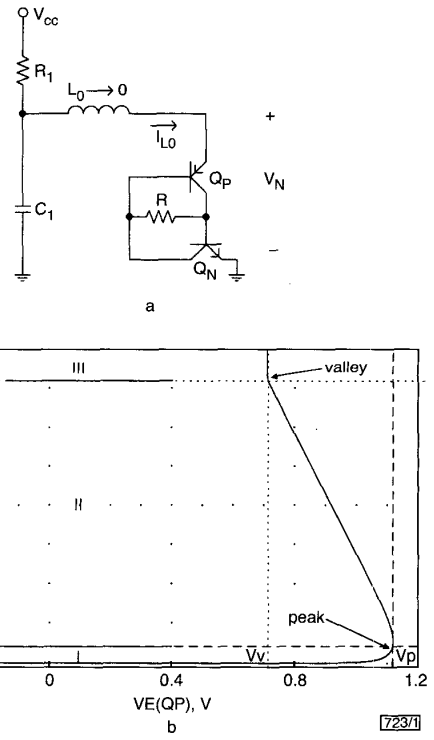

Fig. 1 *Relaxation oscillator and S-shaped nonlinear characteristics*

a Relaxation oscillator
b S-shaped nonlinear characteristics

Relaxation oscillator: Consider the circuit of Fig. 1*a*, where a hysteresis current-controlled nonlinear resistor [5] is coupled directly to a series R_1C_1 timing network supplied by a single voltage supply V_{CC}. The S-shaped characteristic of the nonlinear resistor is shown in Fig. 1*b*. This circuit represents a relaxation oscillator; capacitor C_1 is charged through R_1 until the voltage across the nonlinear resistor reaches its peak V_P (see Fig. 1*b*). At this point, the nonlinear resistor is 'fired' and C_1 discharges rapidly reaching its valley point V_V. The repetition of this action results in a typical sawtooth waveform with a dynamic swing $\Delta V = V_P - V_V$. There-

fore, the smallest supply voltage that can be used for this circuit is $V_{CC} = V_P$ which implies its suitability for low-voltage operation. The average power consumption of the oscillator is equal to $V_{CC}(V_{CC} + V_P - 2V_V)/R_1$.

The following set of equations describes the oscillator:

$$R_1 C_1 \dot{V}_{C1} = V_{CC} - V_{C1} - R_1 I_{L0} \quad (1a)$$

$$L_0 \dot{I}_{L0} = V_{C1} - V_N \quad (1b)$$

where I_{L0} ($I_E(Q_P)$) is the current in the parasitic transit inductor and V_N ($V_E(Q_P)$) is the voltage across the nonlinear resistor, which can be approximated by linear segments as (see the regions indicated in Fig. 1*b*):

$$V_N = \begin{cases} V_P I_{L0}/I_P & 0 \le I_{L0} < I_P \quad \text{Region I} \\ V_P - \frac{V_P - V_V}{I_V - I_P}(I_{L0} - I_P) & I_P \le I_{L0} < I_V \quad \text{Region II} \\ V_V & I_{L0} \ge I_V \quad \text{Region III} \end{cases} \quad (2)$$

By setting $X = VC_1/V_{ref}$, $Z = R_1 I_{L0}/V_{ref}$, $\tau = t/R_1 C_1$, $K = V_{CC}/V_{ref}$, $\Delta = V_V/V_{ref}$, $\beta = R_1^2 C_1/L_0$ and choosing $V_{ref} = 1$, the dimensionless form of the above model becomes

$$\begin{pmatrix} \dot{x} \\ \dot{Z}/\beta \end{pmatrix} = \begin{pmatrix} -1 & -1 \\ 1 & -b\Delta \end{pmatrix} \begin{pmatrix} X \\ Z \end{pmatrix} + \begin{pmatrix} K \\ -a\Delta \end{pmatrix} \quad (3a)$$

and

$$(a, b) = \begin{cases} (0, P_1 P_2/m) & 0 \le Z < m/P_2 \\ (P_1 + \frac{P_1 - 1}{P_2 - 1}, \frac{1 - P_1}{P_2 - 1}\frac{P_2}{m}) & m/P_2 \le Z < m \\ (1, 0) & Z \ge m \end{cases} \quad (3b)$$

The sawtooth waveform obtained via numerical integration of eqn. 3 using an adaptive-step Runge-Kutta algorithm is shown in Fig. 2. The unipolar mode of operation results from using a single positive supply V_{CC}. If required, bipolar signals can be obtained at the expense of using another negative supply.

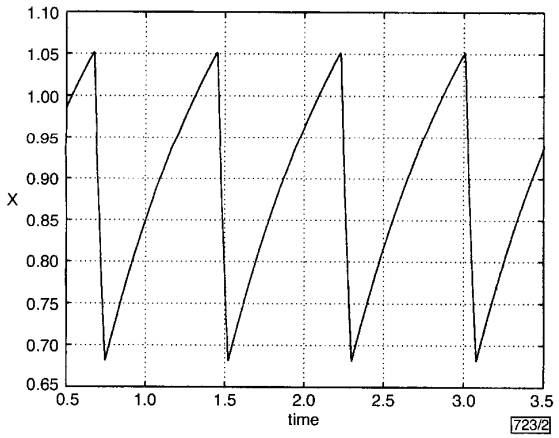

Fig. 2 *Sawtooth waveform from numerical integration of eqn. 3 with K = 1.5, Δ = 0.7, β = 10^{+4}, P_1 = 1.5, P_2 = 50 and m = 5*

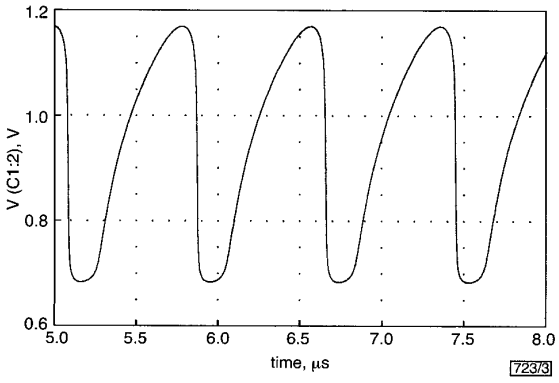

Fig. 3 *Sawtooth from PSPICE simulation with R_1 = 5kΩ, C_1 = 100pF, R = 2kΩ, V_{CC} = 1.5V*

The equilibrium points of eqn. 3 are $(x_0, z_0) = [\Delta/(1+b\Delta)](Kb + a, -a + K/\Delta)$. At these points, the calculated eigenvalues are (–1.095, -10^{+5}) in the region $0 \le Z < m/P_2$, (13.265, 700) in the region $m/P_2 \le Z < m$, and (–2.429, –6999) in the region $Z \ge m$, for the values corresponding to Fig. 2. Therefore, the real equilibrium point in the region $m/P_2 \le Z < m$ is unstable. The normalised frequency of oscillation is $\omega_0 = \sqrt{[\beta(1 + b\Delta)]}$. Note that *a* and *K* do not affect the circuit dynamics; they only move the equilibrium points.

A PSPICE simulation of the oscillator was performed taking R_1 = 5kΩ, C_1 = 100pF, R = 2kΩ, V_{CC} = 1.5V and using a BC559 *pnp* transistor and a Q2N2222 *npn* transistor. The voltage V_{C1} is shown in Fig. 3. The nonlinear characteristic of Fig. 1*b* is also a PSPICE simulation with the same components. With the same values in the simulation, a circuit was constructed. The measured voltage swing was 350mV. We have also confirmed the generation of bipolar signals using dual ±1V supplies.

Conclusion: A simple low-voltage relaxation oscillator has been described. Using commercial bipolar transistors, a single 1.5V supply was sufficient to power the circuit. A lower supply is possible when special transistors with low V_T are used. The circuit is attractive for monolithic implementation; it is inductorless. Including a parasitic inductor into the oscillator's nonlinear model is fundamental to reproducing its dynamics.

2 May 2000
Electronics Letters Online No: 20000958
DOI: 10.1049/el:20000958

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Simplified technique for syllabic companding in log-domain filters

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It is shown that when syllabic companding is applied to log-domain filters using dynamic biasing, their large signal linearity can be exploited to eliminate the state variable compensation circuit. Owing to its simplicity, the proposed technique has several advantages over previous approaches.

Introduction: Fig. 1*a* shows a first-order log-domain filter [1] which is ideally linear and time-invariant (LTI) [1, 2] between the large signal currents i_{1p} and i_{4p} in its input and output transistors (Fig. 1*a*, assuming $i_{1p} > 0$). i_{1p} is the sum of an AC input signal i_{in} and a bias I_{bias}. In traditional implementations, I_{bias} is a constant. The output i_{outp} is obtained by subtracting $(I_2/I_3)I_{bias}$ from i_{4p} as shown in Fig. 1*a* (I_2/I_3 is the DC gain of the filter [1, 2]).

In [3] dynamic biasing is applied to the circuit in Fig.1*a* by varying I_{bias} in accordance with the envelope of the input i_{in} so that I_{bias} is slightly larger than the minimum required value for i_{1p} to stay positive at all times. This lowers the power consumption and the output noise of the filter for small inputs and helps accommodate very large inputs. This also alters the 'gain' from the input