# Motivating Two-Port Network Analysis Through Elementary and Advanced Examples

**Abstract**

**We seek to motivate the use of the not-so-popular two-port network circuit analysis techniques via proposing two examples; one of which is elementary while the other is advanced. In particular, we start by deriving the transmission matrices for small-signal equivalent models of the BJT and MOS transistors. We then proceed to the first example where we explain the function of a Gyrator in a very clear way aided with Spice simulations. In the second more advanced example, we show how to systematically analyze the classical Cascode amplifier in a general way that is independent of whether it is realized using a BJT or an MOS transistor. The two examples highlight the strength and generality of the two-port analysis.**

## I. INTRODUCTION

Two-port network descriptions of circuits are an old yet valuable analysis tool [1], [2]. Traditionally, two-port network representations are applied to analyze complex networks which can be dissolved into sub-networks connected in series, parallel or cascade [3]. Two-port network analysis applies sequentially a series of matrix manipulations (multiplication, addition or inversion); the computational overhead of which depends on the network size and connectivity. Although it is possible to derive two-port matrix representations of individual devices (transistors, op amps, transconductance amplifiers...etc.), this is rarely done as classical mesh/nodal analysis techniques are more dominant. It is also usually the case that students are introduced to two-port networks late in their study which discourages them from using it, as seen from the chapter sequence for example in [3].

Most transistor-based circuits are analyzed using mesh and nodal analysis techniques after recalling a small-signal equivalent circuit of the transistor [4], [5]. If this equivalent circuit is changed by introducing an extra element (impedance, dependent source, noise source...etc.), it is usually necessary to repeat the analysis. Another reason for the not-so-popular two-port network analysis may be historically related to the hybrid $(h)$ parameters which were intentionally introduced to model the Bipolar transistor [3]-[5]. Unlike the impedance matrix $(z)$, the admittance matrix $(y)$ or the transmission matrix $(a)$, which are suitable for analyzing inter-connected networks respectively in series, parallel or cascade, the $(h)$ parameters are not related to any network-interconnect method. Of particular importance are the transmission parameters, which are well-suited for networks with feedback [5], defined as

$$\begin{pmatrix} V_1 \\ I_1 \end{pmatrix} = \begin{pmatrix} a_{11} & a_{12} \\ a_{21} & a_{22} \end{pmatrix} \begin{pmatrix} V_2 \\ -I_2 \end{pmatrix} \tag{1}$$

where $V_{1,2}$ are respectively the input and output two-port network voltages and $I_{1,2}$ are respectively the input and output two-port network currents (see Fig. 1(a)).

In this work, we aim to show the strength and generality of the two-port network analysis techniques via two examples. In particular, the following is presented

1) We start by deriving transmission parameters for simple small-signal equivalent models of BJT and MOS transistors. This is the only step where mesh and nodal analysis need to be applied.
2) An example is given to explain the function of a Gyrator. Spice simulations are given to illustrate this function.
3) Finally, an advanced example is given to derive the expressions for the voltage gain $A_v$, the current gain $A_i$, the input impedance $Z_i$ and output impedance $Z_o$ of a cascode amplifier independent of the type of transistor used. These expressions are then evaluated for BJT and MOS transistors. One can witness that there is a lot of renewed interest in exploring different amplifier analysis techniques [6]-[10].

## II. BJT AND MOS TRANSISTOR TRANSMISSION PARAMETERS

Figure 1(b) shows the small signal equivalent circuit of an NPN BJT transistor operating in the forward active mode. The model comprises two terminal resistors $(r_b, r_e)$ (ideally $r_e = 0$) and a dependent current-controlled current source $\beta I_1$ with output resistance $r_o$. $\beta$ is the forward active current gain (assumed constant) and $r_b$ is

related to the BJT small-signal transconductance $g_m$ as $r_b = \beta/g_m$. It is relatively easy to apply mesh and nodal analysis to this equivalent circuit in order to derive the transmission matrix

$$\begin{pmatrix} a_{11} & a_{12} \\ a_{21} & a_{22} \end{pmatrix} = \frac{-1}{\beta r_o - r_e} \begin{pmatrix} r_b + r_e & \beta r_e r_o + r_b(r_o + r_e) \\ 1 & r_o + r_e \end{pmatrix} \tag{2}$$

Many such examples are given in [3].

The above matrix may be simplified considering that $\beta r_o >> r_e$ and that $(1/\beta r_o) \to 0$ to become

$$\begin{pmatrix} a_{11} & a_{12} \\ a_{21} & a_{22} \end{pmatrix} = \begin{pmatrix} \frac{-1}{g_m r_o} & -(r_e + \frac{1}{g_m} + \frac{r_e}{g_m r_o}) \\ 0 & \frac{-1}{\beta} \end{pmatrix} \tag{3}$$

If $g_m r_o$ is sufficiently large (which is usually true), a further simplification yields

$$\begin{pmatrix} a_{11} & a_{12} \\ a_{21} & a_{22} \end{pmatrix} = - \begin{pmatrix} 0 & r_e + \frac{1}{g_m} \\ 0 & \frac{1}{\beta} \end{pmatrix} \tag{4}$$

In a similar manner, and recalling the small signal equivalent circuit of a MOS transistor operating in the saturation mode (Fig. 1(c)), it can be shown that the $(a)$ matrix for this circuit is

$$\frac{-1}{g_m r_{ds}} \begin{pmatrix} 1 & r_s(1 + g_m r_{ds}) + r_{ds} \\ 0 & 0 \end{pmatrix} \approx \begin{pmatrix} \frac{-1}{g_m r_{ds}} & -(r_s + \frac{1}{g_m}) \\ 0 & 0 \end{pmatrix} \tag{5}$$

where $g_m$ is the small signal transconductance, $r_{ds}$ is the drain to source resistance and $r_s$ is the source resistance (ideally $r_s = 0$). More comprehensive models which take into consideration parasitic capacitors can also be derived. Consider for example the MOS transistor small signal model of Fig. 1(d) where an impedance $Z$ (maybe a parasitic $C_{gd}$ capacitor for example or an external impedance) is connected from gate to drain. The transmission matrix in this case can be shown to be

$$\frac{r_{ds}(1 + g_m r_s)}{r_{ds}(1 - g_m Z) + r_s} \begin{pmatrix} 1 + \frac{Z}{r_{ds}(1+g_m r_s)} & Z \\ \frac{1}{r_{ds}} \frac{1+g_m r_{ds}}{1+g_m r_s} & 1 \end{pmatrix} = \frac{1}{1 - g_m Z} \begin{pmatrix} 1 & Z \\ g_m & 1 \end{pmatrix}_{r_{ds}=\infty, r_s=0} \tag{6}$$

However, the design procedure for most application circuits is usually based on the simplified small-signal BJT and MOS equivalent circuits (Figs. 1(b) and 1(c)) and the corresponding device equations reflected by (4) and (5).

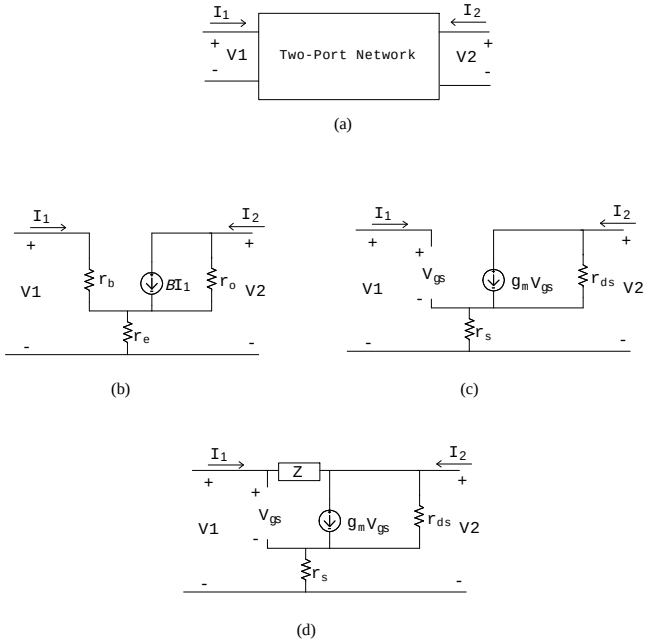



Figure 1: (a) Two-port network variables; (b) basic small signal equivalent model of a BJT transistor; (c) basic small signal equivalent model of a MOS transistor and (d) MOS transistor model with a gate-to-drain impedance $Z$.

## III. Gyrator Example

It is seen from (4) and (5) that the difference in device characteristics between the BJT and MOS transistors can be summarized in a *Null* first column (for the BJT) and a *Null* second row (for the MOS) in their transmission matrices. The corresponding ideal equivalent circuits are shown in Fig. 2. However, matrix mutation implies the existence of two other alternative devices as direct counterparts. These two devices should have the two transmission matrices

$$\begin{pmatrix} a_{11} & 0 \\ a_{21} & 0 \end{pmatrix} \quad \text{and} \quad \begin{pmatrix} 0 & 0 \\ a_{21} & a_{22} \end{pmatrix} \tag{7}$$

A question may be raised to students as to how is it possible to obtain such devices? The answer is by using a gyrator. Traditionally, a gyrator is explained to students via the classical example of converting a capacitance into an inductance. Via cascading a gyrator, a grounded capacitor and another gyrator, as shown in Fig. 3, one obtains

$$\begin{pmatrix} 0 & r \\ \frac{1}{r} & 0 \end{pmatrix} \begin{pmatrix} 1 & 0 \\ cS & 1 \end{pmatrix} \begin{pmatrix} 0 & r \\ \frac{1}{r} & 0 \end{pmatrix} = \begin{pmatrix} 1 & Scr^2 \\ 0 & 1 \end{pmatrix} \tag{8}$$

which is equivalent to and inductor with inductance $L = r^2C$; $r$ being the gyration resistance. A typical op amp implementation of the gyrator [11] is also usually given.

However, in our example, we want to show the student how a gyrator can be used to invert the characteristics of a BJT or MOS transistor. In particular, cascading a BJT and a gyrator yields a device whose transmission matrix has a *Null* second column instead of a *Null* first column

$$\begin{pmatrix} 0 & -(r_e + \frac{1}{g_m}) \\ 0 & \frac{-1}{\beta} \end{pmatrix} \begin{pmatrix} 0 & r \\ \frac{1}{r} & 0 \end{pmatrix} = \begin{pmatrix} -\frac{r_e + \frac{1}{g_m}}{r} & 0 \\ -\frac{1}{r\beta} & 0 \end{pmatrix} \tag{9}$$

This device maybe termed the gyrated-BJT (G-BJT) whose equivalent circuit is also shown in Fig. 2 and is seen to represent a voltage-controlled voltage-source.

Now cascading a gyrator followed by a MOS transistor would yield a device whose transmission matrix has *Null* first row instead of a *Null* second row

$$\begin{pmatrix} 0 & r \\ \frac{1}{r} & 0 \end{pmatrix} \begin{pmatrix} \frac{-1}{g_m r_{ds}} & -(r_s + \frac{1}{g_m}) \\ 0 & 0 \end{pmatrix} = \begin{pmatrix} 0 & 0 \\ \frac{-1}{r g_m r_{ds}} & \frac{r_s + \frac{1}{g_m}}{-r} \end{pmatrix} \tag{10}$$

This device maybe termed the gyrated-MOS (G-MOS) whose equivalent circuit is also shown in Fig. 2. Compared to the MOS transistor ; the G-MOS represents a current-controlled-current-source instead of a voltage-controlled current-source.

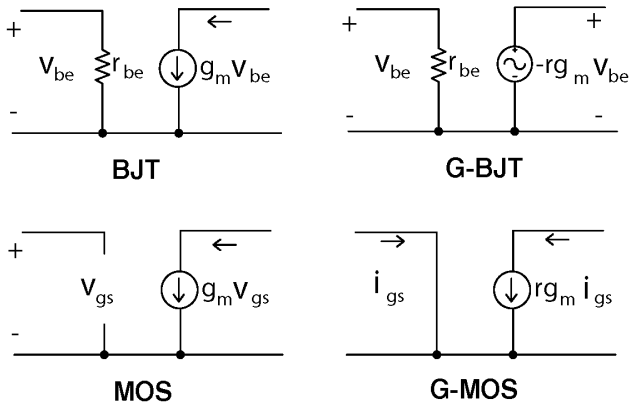



Figure 2: Equivalent circuits of the G-BJT and G-MOS compared to the BJT and MOS transistors.

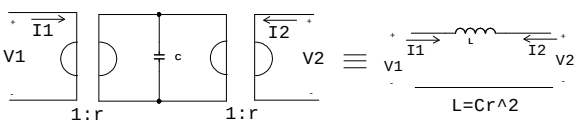



Figure 3: Classical gyrator application in realizing a floating inductor.

### A. Spice modelling and simulations

We demonstrate here an application of both the G-BJT and G-MOS devices. In particular, recalling the equivalent circuit of G-BJT shown in Fig. 2 suggests that connecting a voltage source $V_s$ to the input of the device ($V_s = V_{be}$) and assuming the source resistance is negligible yields an open-circuit output voltage which equals $-g_m r V_s$. Hence, without need for a load impedance, this device inherently operates as an inverting voltage amplifier with gain $A_v = -g_m r$. Figure 4(a) shows a simple Spice implemented circuit verifying this structure where two ideal VCCS blocks (Spice $G$ blocks) labelled G-gyrator1 and 2 are used to construct a gyrator with $r = 1k\Omega$. Another ideal VCCS (labelled G-BJT) is used to model a BJT with $g_m = 10mA/V$. Hence, the cascade connection yields a voltage gain of $-10$ as confirmed in Fig. 5(a). Both $g_m$ and $r$ are set internally as VCCS Spice parameters.

For the G-MOS, the application of a current integrator is illustrated in Fig. 4(b) where an input square-wave current source $I_s$ is integrated by connecting an RC network directly to the output of the G-MOS. Simulation results are shown in Fig. 5(b) for $g_m = \frac{1}{r} = 1mA/V$, $R_{out} = 10k\Omega$ and $C_{out} = 10nF$.

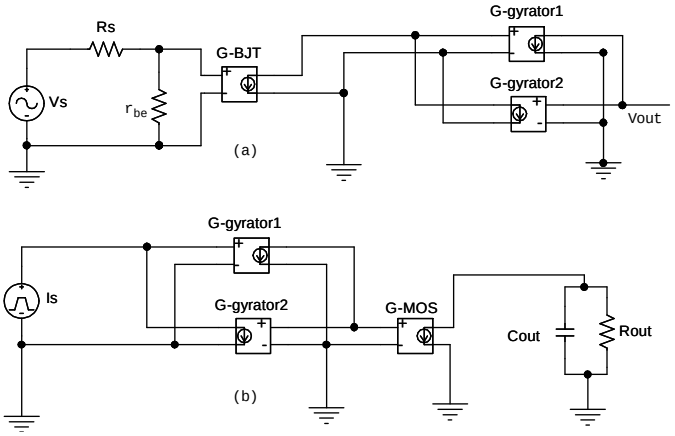



Figure 4: Circuits used to simulate (a) a voltage amplifier using the G-BJT and (b) a current integrator using the G-MOS.

## IV. Cascode Amplifier Example

The composite cascode amplifier is classically formed of a two-stage common-(emitter/source) common-(base/gate) cascade. Due to the very low input impedance of the common-(base/gate) stage, the gain of the first stage drops significantly and hence reduces the value of the Miller capacitance thus increasing the bandwidth. The gain is then recovered by the second stage [12]-[13]. The analysis of the cascode amplifier using mesh and nodal analysis usually poses difficulty to the student when the two transistors are directly replaced with their equivalent circuits. Difficulty increases when parasitic capacitors are considered as part of the equivalent circuit. Of course, without considering these parasitics, the purpose of utilizing a cascode amplifier becomes unclear.

Here, we propose using the two-port representation of the cascode amplifier, shown in Fig. 6. Assuming two identical transistors, the amplifier can be modelled by the two equations

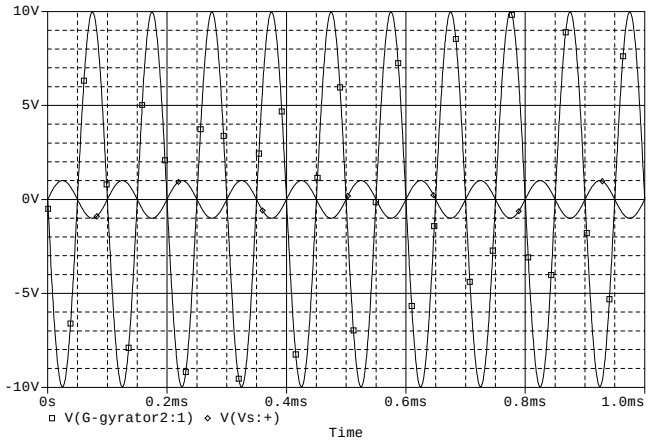
$$\begin{pmatrix} V_s - I_i R_s \\ I_i \end{pmatrix} = \begin{pmatrix} a_{11} & a_{12} \\ a_{21} & a_{22} \end{pmatrix} \begin{pmatrix} V_2 \\ -I_2 \end{pmatrix} \tag{11a}$$

$$\begin{pmatrix} -V_2 \\ I_o - I_L - I_2 \end{pmatrix} = \begin{pmatrix} a_{11} & a_{12} \\ a_{21} & a_{22} \end{pmatrix} \begin{pmatrix} V_o - V_2 \\ I_o - I_L \end{pmatrix} \tag{11b}$$

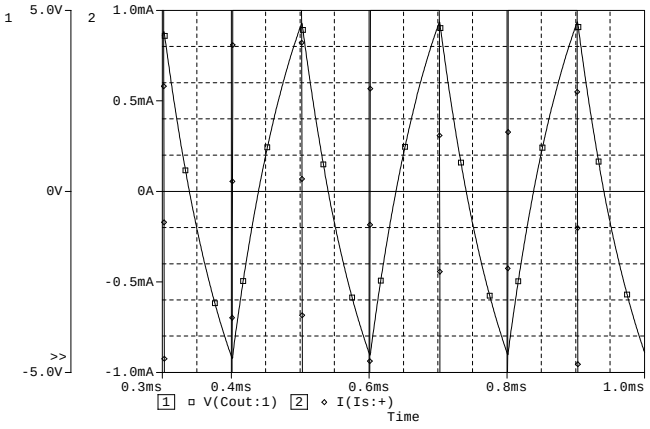
where $V_s$ is the source voltage with internal resistance $R_s$, $I_i$ is the current drawn from this source, $V_o$ is the output voltage, $I_o$ is the output current (see Fig. 6), $I_L$ is the current in the load ($I_L = V_o/Z_L$), $V_2$ and $I_2$ are as indicated in Fig. 6 the output voltage and output current of the first-stage (common-(emitter/source)). Note that the input voltage of the second-stage (common-(base/gate)) is $-V_2$ and its input current is $I_2 - I_4 = I_2 - I_o + I_L$. Readers interested in exploring more examples on two-port modeling of amplifiers can refer to [14].

From the above equations, the expressions in Table 1 of the four important design variables of the cascode amplifier can be systematically derived. These expressions are written for simplicity as functions of $\Delta_1 = (a_{11} + \frac{a_{12}}{Z_L})/(a_{11} - 1)$, $\Delta_2 = (\frac{a_{21}+(a_{12}a_{21}/Z_L)}{a_{11}-1} - \frac{1+a_{22}}{Z_L})$ and $\Delta_3 = \frac{a_{11}+a_{21}R_s}{a_{12}+a_{22}R_s} - a_{21}$. The derivation process is an excellent exercise for students where the voltage gain is defined as $A_v = (V_o/V_s)|_{I_o=0}$, the input impedance is defined

as $Z_i = (V_s/I_i)|_{I_o=0}$, the current gain is defined as $A_i = (I_o/I_i)|_{V_o=0}$ and the output impedance is defined as $Z_o = (V_o/I_o)|_{V_s=0}$.




(a)




(b)

Figure 5: Spice simulation results of (a) the voltage amplifier of Fig. 4(a) wih gain $-10$ ($R_s = 50\Omega$, $r_{be} = 20k\Omega$) and (b) the current integrator of Fig. 4(b).

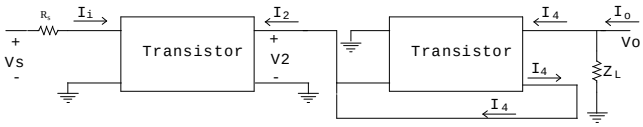



Figure 6: Two-port representation of the Cascode amplifier.

It now remains to evaluate these expressions when BJT or MOS transistors are used. Substituting with (4) and (5) the in Table 1 yields the simplified expressions in Table 2 in the two cases that the cascode amplifier is implemented using BJT or MOS transistors at $R_s = 0$.

An alternative interesting amplifier can also be obtained if we for example use the MOS transistor model shown in Fig. 1(d), where $Z$ is an external gate-to-drain impedance, and described by the matrix (6). The cascode amplifier design parameters in this case are as given in Table 3 at $Z_L = \infty$.

It is very important here to note that by using two-port network parameters, any change in the transistor model or equivalent circuit does not imply a need to re-analyze the amplifier and derive different expressions for its four design parameters. The only thing that would be needed is to derive the new transmission matrix and then substitute with its elements in the Tables. Although we have given here the example of a cascode amplifier, many other examples can be found in [14]. Not only that, but the use of two-ports can even be extended to provide general characteristic equations for many other circuits such as oscillators for example [15].

| | | |
|---|---|---|
| $A_v$ | general | $\frac{1}{(a_{11}+a_{21}R_s)\Delta_1-(a_{12}+a_{22}R_s)\Delta_2}$ |
| | at $R_S$=0 | $[\frac{a_{11}(a_{11}+\frac{a_{12}}{Z_L})-a_{12}a_{21}(1+\frac{a_{12}}{Z_L})}{a_{11}-1}+\frac{a_{12}(1+a_{22})}{Z_L}]^{-1}$ |
| $Z_i$ | general | $\frac{1}{A_v(a_{21}\Delta_1-a_{22}\Delta_2)}$ |
| | at $R_S$=0 | $\frac{(a_{11}-1)/A_v}{a_{21}(a_{11}+\frac{a_{12}}{Z_L})\text{-}a_{22}(a_{21}+\frac{a_{12}a_{21}+(1+a_{22})(1-a_{11})}{Z_L})}$ |
| $Z_o$ | general | $\frac{(1+a_{22}+\frac{a_{12}\Delta_3}{a_{11}-1})}{a_{21}+\Delta_1\Delta_3+\frac{1+a_{22}}{Z_L}}$ |
| | at $R_S$=0 | $\frac{(1+a_{22})(a_{11}-1)+a_{11}-a_{12}a_{21}}{(\frac{a_{11}}{a_{12}}-a_{21})(a_{11}+\frac{a_{12}}{Z_L})+(a_{11}-1)(a_{21}+\frac{1+a_{22}}{Z_L})}$ |
| $A_i$ | general | $-[a_{22}(\frac{a_{12}a_{21}(1-a_{22})}{a_{22}(1-a_{11})}-a_{22}-1)]^{-1}$ |
| | at $R_S$=0 | independent of $R_s$ |

Table 1: Important parameters derived for the cascode amplifier

| Parameter | BJT | MOS |
|---|---|---|
| $A_v$ | $\frac{Z_L}{a_{12}(1+a_{22})}$ $\approx -g_m Z_L\vert_{r_e=0}$ | $[\frac{a_{11}(a_{11}+\frac{a_{12}}{Z_L})}{a_{11}-1}+\frac{a_{12}}{Z_L}]^{-1}$ $\approx -g_m Z_L\vert_{r_{ds}=\infty,r_s=0}$ |
| $R_i$ | $\frac{1}{A_v}\frac{Z_L}{a_{22}(1+a_{22})}$ $\approx \beta/g_m\vert_{r_e=0}$ | $\infty$ |
| $R_o$ | $Z_L$ | $\frac{(a_{11}-1)+a_{11}}{\frac{a_{11}}{a_{12}}(a_{11}Z_L+a_{12})+a_{11}-1}Z_L$ $=\frac{2+g_m r_{ds}}{2+g_m r_{ds}+(Z_L/r_{ds})}Z_L$ $\approx Z_L$ |
| $A_i$ | $[\frac{1}{\beta}(\frac{1}{\beta}-1)]^{-1}$ $\approx -\beta$ | $\infty$ |

Table 2: Cascode amplifier design practical parameters

| | |
|---|---|
| $A_v$ | $[\frac{\frac{1}{g_m}(\frac{1}{Z}+\frac{1}{Z_L})-1-\frac{Z/Z_L}{(1-g_m Z)}}{(1-g_m Z)}+\frac{2Z/Z_L}{(1-g_m Z)^2}]^{-1}\approx g_m Z$ |
| $Z_i$ | $\infty$ |
| $Z_o$ | $Z\frac{1-A_v^2}{1-2A_v+A_v^2}$ |
| $A_i$ | $\frac{1-A_v}{2}$ |

Table 3: Parameters of an alternative cascode amplifier using the equivalent circuit in Fig. 1(d)

## V. CONCLUSION

The not-so-popular two-port network analysis techniques are extremely useful and should be motivated in teaching Electronics. The particular advantages of employing these techniques include:

1) deriving only once expressions which are independent of the complexity of the transistor (or op amp) model. This saves a lot of time.
2) making use of inter-network connectivity. Simple or complex networks can always be split into series, parallel or cascade interconnects. Special case matrices can be written straight away. For example, a grounded impedance has the transmission matrix $\begin{pmatrix} 1 & 0 \\ 1/Z & 1 \end{pmatrix}$ while a floating one has the transmission matrix $\begin{pmatrix} 1 & Z \\ 0 & 1 \end{pmatrix}$.

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